

# How to build a GPU cluster

Christopher Milan

AI Safety at UCLA

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- These slides will be available online at [ais-ucla.org/~chris](http://ais-ucla.org/~chris).

# What is this talk about?

While setting up and administrating our servers, I ran into many interesting challenges.

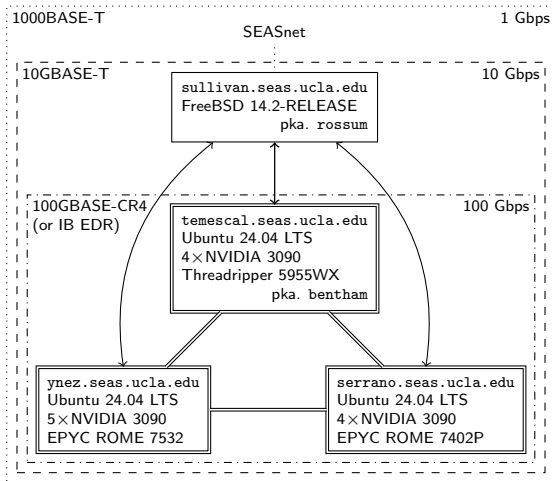
This talk will focus on how we chose our hardware.

There are many other interesting things to learn from this cluster, check out our blog.<sup>1</sup>

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<sup>1</sup>[blog.aisafetyatucla.org](http://blog.aisafetyatucla.org)

# Server topology



# Why AMD (EPYC ROME)?

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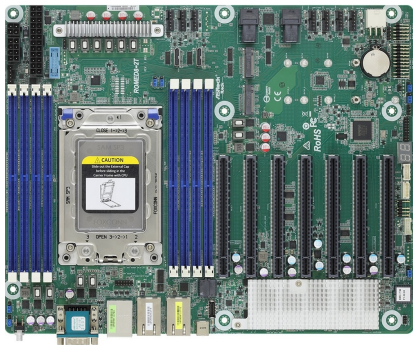
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- PCIe lanes:

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AMD's "Zen 2" server CPUs.

- Memory bandwidth: 8 channels of DDR4-3200, roughly 200GB/s.
- Price: A 7532 is about \$200 on ebay.
- PCIe lanes: EPYC ROME has **128 PCIe 4.0 lanes**.

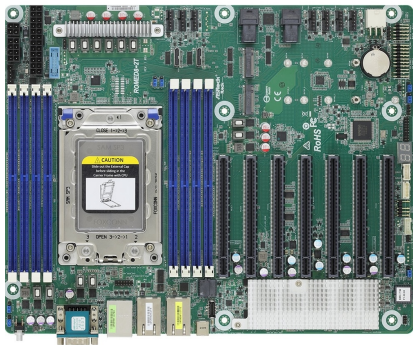
# ROMED8-2T



- Reasonably priced (at the time...)

Figure: ASRock Rack ROMED8-2T

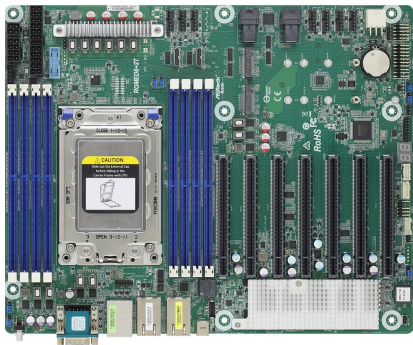
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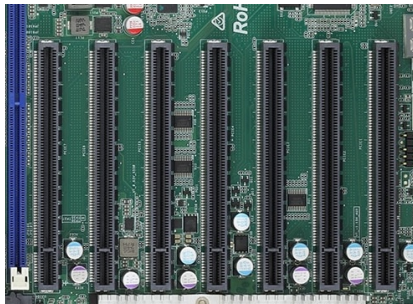


Figure: ROMED8-2T PCIe slots

- Reasonably priced (at the time...)
- 7×PCIe 4.0x16 (but slot #2 is cursed)
- The slots are too close!

# PCIe risers to the rescue!

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- Crypto miners have this exact same problem
- Solution: PCIe risers
- Surely nothing could go wrong...



Figure: PCIe risers on temescal

# Signal integrity errors

```
73.837122] snd_hda_intel 0000:c2:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.837544] snd_hda_intel 0000:c2:00.1: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.837964] nvldia 0000:81:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.838384] nvldia 0000:81:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.838804] snd_hda_intel 0000:81:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.839225] snd_hda_intel 0000:81:00.1: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.839647] nvldia 0000:46:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.840065] nvldia 0000:46:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.840487] snd_hda_intel 0000:46:00.1: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
**] A start job is running for Wait for Network to be Configured (min 7s / no limit)
73.464217] pciexpress 0000:40:03.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.465474] pciexpress 0000:40:03.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.465569] pciexpress 0000:00:01.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.467627] pciexpress 0000:00:01.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.468986] pciexpress 0000:40:03.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.469746] pciexpress 0000:40:03.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.470798] pciexpress 0000:00:01.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.471842] pciexpress 0000:00:01.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.472301] pciexpress 0000:40:03.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.473377] pciexpress 0000:40:03.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.474333] pciexpress 0000:00:01.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.476201] pciexpress 0000:00:01.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.477071] pciexpress 0000:40:03.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.478107] pciexpress 0000:40:03.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.479150] pciexpress 0000:00:01.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.480194] pciexpress 0000:00:01.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.481239] pciexpress 0000:00:01.1: AER: aer_status: 0x00000100, aer_mask: 0x00000000
73.482283] pciexpress 0000:40:03.1: AER: aer_layer=Data Link Layer, aer_agent=Transmitter ID
73.483298] pciexpress 0000:40:03.1: AER: aer_status: 0x00000100, aer_agent=Transmitter ID
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73.489251] nvldia 0000:c2:00.0: AER: aer_status: 0x00000001, aer_mask: 0x00000000
73.410323] nvldia 0000:c2:00.0: AER: aer_status: 0x00000001, aer_mask: 0x00000000
73.411302] snd_hda_intel 0000:c2:00.1: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.412273] nvldia 0000:81:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.413250] nvldia 0000:81:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.414233] snd_hda_intel 0000:81:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.415213] snd_hda_intel 0000:81:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.416195] nvldia 0000:46:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.417175] nvldia 0000:46:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.418155] snd_hda_intel 0000:46:00.0: AER: aer_status: 0x00000001, aer_agent=Receiver ID
73.419135] nvldia 0000:01:00.0: AER: aer_status: 0x00000001, aer_mask: 0x00000000
73.420115] nvldia 0000:01:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.421095] nvldia 0000:01:00.0: AER: aer_status: 0x00000001, aer_mask: 0x00000000
73.422075] nvldia 0000:01:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
73.423055] nvldia 0000:01:00.0: AER: aer_status: 0x00000001, aer_mask: 0x00000000
73.424035] nvldia 0000:01:00.0: AER: aer_layer=Physical Layer, aer_mask: 0x00000000
```

Figure: AER errors, image from Nathan Odle



# Signal integrity errors

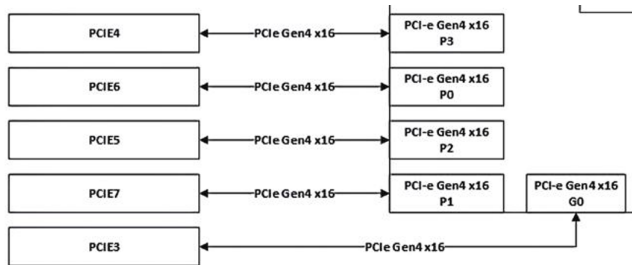


Figure: PCIe slots on ROMED8-2T

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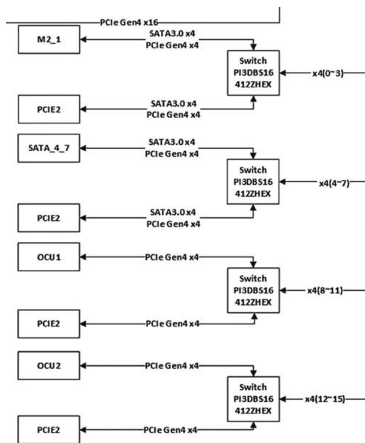
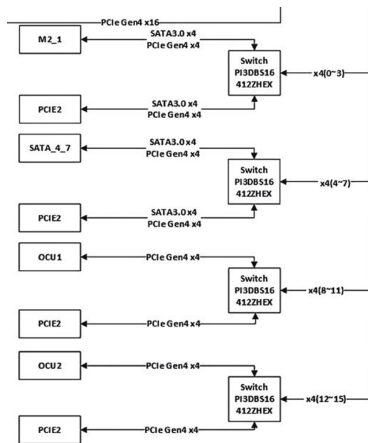


Figure: Remember slot 2? This is him now



# Signal integrity errors



All this switching causes signal loss!

Similarly, adding risers does too.

Figure: Remember slot 2? This is him now

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Why is this a problem? Because at 350W/ea. one power supply is not enough for 6 GPUs.

Taping off the PCIe slot power just causes the cards to fail to be recognized.

# How to fix this?

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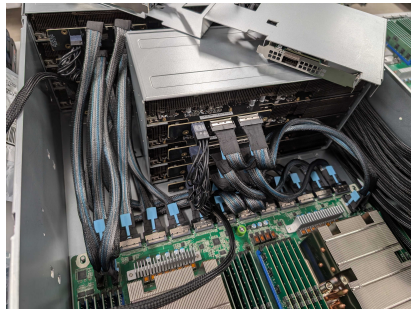


Figure: SlimSAS/MCIO connectors

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However, **we only get one try**.

Visit our website at [ais-ucla.org](https://ais-ucla.org).

Some programs we run:

- Intro to AI Safety Fellowship ([ais-ucla.org/fellowships](https://ais-ucla.org/fellowships)).
- Upskilling Tracks ([ais-ucla.org/upskilling-tracks](https://ais-ucla.org/upskilling-tracks)).
- Reading Group (ask Will).
- Server access (ask me).